



FORM PTO-1083

JUN 30 2004

\$

The application of T. SASAKI et al
Serial No.: 10/073,312

Filed: February 13, 2002

PATENT

Case Docket No. ASA-1062

Group Art Unit: 2825

Examiner: M. Dimyan

For: DESIGN METHOD AND SYSTEM FOR SEMICONDUCTOR INTEGRATED CIRCUITS

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment in the above-identified application.

Small entity status of this application under 37 CFR 1.9 and 1.27 has been established by a verified statement previously submitted.

A verified statement to establish small entity status under 37 CFR 1.9 and 1.27 is enclosed.

No additional fee is required.

The fee has been calculated as shown below:

	(COL. 1)		(COL. 2)		(COL. 3)
Total	* 15	Minus	** 20	=	0
Indep.	* 5	Minus	*** 5	=	0
<input type="checkbox"/> First Presentation of Multiple Dependent Claims					

SMALL ENTITY

Rate	Additional Fee
x 9	\$
x 42	\$
+ 140	\$
Total	\$

OR

OTHER THAN A SMALL ENTITY

Rate	Additional Fee
x 18	\$ 0
x 84	\$ 0
+ 280	\$ 0
Total	\$ 0

* If the entry in Col. 1 is less than the entry in Col. 2, write '0' in Col. 3.
** If the 'Highest Number Previously Paid For' IN THIS SPACE is less than 20, write '20' in this space.
*** If the 'Highest Number Previously Paid For' IN THIS SPACE is less than 3, write '3' in this space.
The 'Highest Number Previously Paid For' (Total or Independent) is the highest number found from the equivalent box in Col. 1 of a prior Amendment or the number of claims originally filed.

Please charge my Deposit Account No. 50-1417 in the amount of \$ _____.

A check in the amount of \$ _____ is attached in payment of: _____.

The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 50-1417.

Any filing fees under 37 CFR 1.16 for the presentation of extra claims.

Any patent application processing fees under 37 CFR 1.17.

Any Extension of Time fees that are necessary, which are hereby requested if necessary.

MATTINGLY, STANGER & MALUR, P.C.
1800 Diagonal Rd., Suite 370
Alexandria, Virginia 22314
(703) 684-1120

Date: June 30, 2004

By:

Daniel J. Stanger
Registration No. 32,846
Attorney for Applicant(s)



1/FW 2825

JUN 30 2004

ASA-1062

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

T. SASAKI et al

Serial No. 10/073,312

Group Art Unit: 2825

Filed: February 13, 2002

Examiner: M. Dimyan

For: DESIGN METHOD AND SYSTEM FOR
SEMICONDUCTOR INTEGRATED CIRCUITS

REPLY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the Office Action mailed March 30, 2004,
please amend the above-identified application as follows. A
certified copy of Japanese priority Patent Application No.
2001-038678 accompanies this Reply in satisfaction of the
requirement set forth in 35 U.S.C. §119.

IN THE TITLE

Please amend the title of the invention to --DESIGN
METHOD AND SYSTEM FOR ACHIEVING A MINIMUM MACHINE CYCLE FOR
SEMICONDUCTOR INTEGRATED CIRCUITS--.